PAUL S DAVID

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PROFILE:

Experienced Device Engineer with a demonstrated history of working in the power semiconductor industry. Skilled in device engineering, characterization, process integration, and management. Proven expertise in devising and implementing solutions to optimize performance, process, and reliability by electrical characterization. Adept at collaborating with cross-functional teams and providing valuable insights for process improvement and product development. Proficient in data analysis of various data sets to provide data driven guidance.

EMPLOYMENT:

Wolfspeed — Durham, NC
Product Engineer - Manufacturing — December 2023 – Present

- Responsible for leading a high impact design change which would result in a substantial decrease in product defectivity and increase device robustness to switching stresses.
- Proposed various projects for Yield and Quality improvements by analyzing real-world performance data and studying workflow processes.
- Compiled weekly KPI report related to complete power product portfolio manufacturing performance.
- Owned and monitored two highest volume Automotive MOSFETs at North Carolina Fab, resolving fabrication, yield and quality issues.

NexGen Power Systems — Santa Clara, CA & Syracuse, NY
Sr. Staff Device Characterization Engineer - Process Integration — January 2021 – December 2023

- Setup and training of electrical characterization equipment for packaged and wafer level devices for product, device & integration engineering teams leading to fast cohesive cycles of learnings from bare wafer to application modules.
- Managed and mentored technicians & junior engineers to perform accurate routine wafer characterization ensuring >90% utilization and high engineering data throughput.
- Oversaw ~0% down time operation and maintenance of >$300k in test equipment and implemented strategic upgrades to align engineering capabilities with company goals.
- Managed process module development of 1200V device portfolio to improve manufacturability and yield.
- Analyzed large electrical wafer sort data and inline fab data to drive yield improvement & correlated electrical parameters to process experiments for product performance improvements.
- Worked extensively in Process Integration team to investigate device physics related phenomenon affecting transistor performance and reliability by developing non-standard characterization tests.
- Achieved multiple device performance milestones by rigorous analysis of metrology and electrical characterization data & collaborating with epi, process, reliability & device engineering teams.
- Completely digitized and automated in-house business processes using productivity tools such as MS Power Automate to improve data organization, access and traceability.

GV Semiconductors — San Jose, CA
Senior Device Engineer — January 2019 –December 2020

- Setup and maintained electrical characterization lab for GaN HEMT power transistors products in wafer and packaged form.

- Performed advanced and standard measurements (such as RDS(on), Gate Charge, Capacitance, etc.) on GaN based D-mode and E-mode devices for deeper understanding of device behavior, parameter extraction and modelling.
- Contributed by providing characterization, layout, and process feedback of GaN based devices leading to improved reliability and performance.
- Contributed to reliability testing of GaN devices crucial to device qualification for mass production.
- Achieved expansion of in-house characterization capabilities by design and implementation of specialized fixtures/techniques while saving company >90% cost of readily available solutions.
- Acted as a liaison between application, technical marketing and fab teams to drive customer-centric product improvements.
- Developed techniques related to Gate Charge measurement of power devices in sub nC range and an alternative method without the use of a current limiting FET.

EDUCATION:

College of Nanoscale Science and Engineering, SUNY Polytechnic Institute Albany, NY
Master of Science in Nanoscale Engineering, Completed May 2017
GPA: 3.68, Concentrating in Nanoelectronics

College of Nanoscale Science and Engineering, University at Albany Albany, NY
Bachelor of Science in Nanoscale Engineering, Completed May 2014
GPA: 3.40, Concentrating in Energy and Environmental Applications

EDUCATIONAL RESEARCH EXPERIENCE:

College of Nanoscale Science and Engineering, University at Albany Albany, NY
Summer Internship, June 2013- August 2013
Project: **$ZnO_{1-x}S_x$ as an Alternative Buffer Layer for CIGS Thin Film Photovoltaics**

College of Nanoscale Science and Engineering, University at Albany Albany, NY
Capstone Project, August 2013- May 2015
Project: **Effect of CVD growth parameters on Electronic and Physical properties of Carbon Nanotubes**

College of Nanoscale Science and Engineering, SUNY Polytechnic Institute Albany, NY
Masters/PhD Project, May 2015- October 2018
Project: **Fabrication and electrical characterization of DNA based PN Diode**

SOFTWARE SKILLS:

- Layout Editor
- Object Oriented Programming
- Power Automate (MS)
- Lab View Programming
- JMP Data Analysis and Scripting
- ACS Basic, Clarius, EasyTest Expert, EasyTest Navigaton
- Spotfire

CHARACTERIZATION AND PROCESSING SKILLS:

- Microfabrication Processes (E-Beam Lithography, deposition, etch, clean)
- Advanced parameter extraction
- AC-DC Measurements on wafer and packaged devices
- Failure Analysis (SEM, TEM, AFM, EDX)
- Wafer Prober measurement (Manual/Automated)
- Dynamic Measurements (Ciss, Coss, Crss, Rg)
- Physical and Chemical Vapor Deposition
- Electrical Parameter Analyzer (4200, B1505/6)
- Gate charge measurements